

## Re: Reading serial port lines

**Source:** <http://coding.derkeiler.com/Archive/Delphi/comp.lang.pascal.delphi.misc/2004-10/0499.html>

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**From:** David Reeve (*dree4456\_at\_big-pond.net.au*)

**Date:** 10/14/04

Date: Thu, 14 Oct 2004 08:51:52 GMT

"L D Blake" <not@any.adr> wrote in message  
news:jfkrm0hhfbo2bnnmp3fjeq0s35nsd2oui8@4ax.com...  
> *On Thu, 14 Oct 2004 00:49:31 GMT, "David Reeve" <dree4456@big-pond.net.au>*  
> *wrote:*  
>  
> *>Errr....logic thresholds have everything to do with it, this is a real*  
*world*  
> *>logic device we are talking about. Start to think about a formal*  
*engineering*  
> *>description of the situation and you'll see what I mean.*  
>  
> *David,*  
> *In a peripheral way logic levels do matter... but I seriously doubt it's*  
*much*  
> *of an issue when you have a capacitor being discharged every time the*  
*switch*  
> *bounces closed and charging only a few millivolts while it's bounced open.*  
>  
> *Remember, we are talking about an event that might last less than a*  
*hundredth*  
> *of a second... with perhaps a dozen or so sub-events lasting only a couple*  
*of*  
> *milliseconds each. It's not like we are putting a logic gate into long*  
*term*  
> *abiguity and, given that most IO driver chips now use schmidt inputs they*  
*are*  
> *hysteresis guarded to begin with.*  
>  
> *I've done this hundreds of times on some pretty groddy switches and it's*  
*never*  
> *been a problem yet.*  
>

I think we are comparing 'what you can get away with' versus good engineering practice. To get back to programming, an analogous situation is to be found in how well one engineers the interaction between the components of a multithreaded environment. We could both agree that a race hazard

exists, but differ markedly in terms of whether it is likely to come and bite us. When designing electronics for a production environment, or designing software for commercial release, I refuse to be impressed by the argument 'well it works doesn't it' . To my mind it must be demonstrably correct by design and calculation, including multiple belts and braces where adequate theory can't be found.

Dave