

Re: What is the Best PCB Layout software ? (Money no object)

Source: <http://coding.derkeiler.com/Archive/General/comp.arch.embedded/2004-01/0931.html>

From: Kay Schubert (*kaytastroph_at_gmx.de*)

Date: 01/13/04

Date: Tue, 13 Jan 2004 10:52:18 +0100

Ralph,

try to use polygones. Don't forget to give it/them the right signal name. If the signal name (e.g. GND) is the same for different polygones or Vias, Eagle will connect them together (or tries it). I hope it helps you....

...kay

"Ralph Malph" <noone@yahoo.com> schrieb im Newsbeitrag
news:40037BCE.9A6DFF99@yahoo.com...

> *Ralph Malph wrote:*

>>

>> *Ian McBride wrote:*

>>>

>>> *"Ralph Malph" <noone@yahoo.com> wrote in message*

>>> *news:40036859.F8EA05E7@yahoo.com...*

>>>>

>>>> *One thing it can't do (without screwing up the DRC) is holes in a
PAD.*

>>>> *I am using a small regulator that requires heat spreaders on the top
and*

>>>> *bottom of the board connected by vias directly under the thermal pad
on*

>>>> *the bottom of the package. I know this is not normal, but TI
recommends*

>>>> *it. I was never able to get rid of the DRC errors this produced.*

>>>>

>>>> *If this is the package I remember, you can make the thermal pad a
small pad*

>>>> *with THERMAL=OFF inside a rectangle on the top layer. A pain, but no
DRC*

>>>> *complaints.*

>>>>

>>>> *I am not trying to make a thermal. I am trying to make a fairly large*

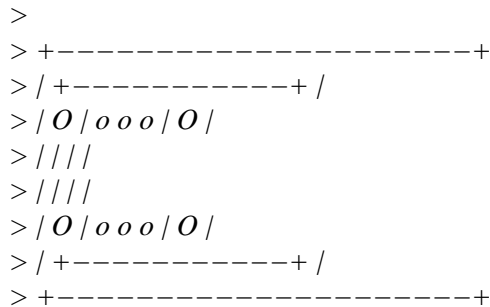
>>>> *rectangular pad with six holes (vias) in it. The entire rectangle needs*

>>>> *to have the solder mask removed from it. I guess I could have split the*

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> > pad up into six equal, rectangular areas as pads. But they should be
> > touching and I don't think I can get this past the DRC either unless I
> > allow everything to touch. I believe I have object spacing set for 10
> > mil at the moment.
> >
> > Or could I use a polygon to open up an area in the solder mask? I did
> > not try much in that area.
>
> By George! That did it! I can draw a rectangle on the tStop layer to
> open up some copper around the six pads. I already found somewhere that
> you can put the same name on multiple pads by adding a \$ or # or
> something similar to the name. So I could use six pads inside a solder
> mask rectangle to add these to the part.
>
> However, there are still four more vias that are outside this pad area
> that need a surface plane which is under solder mask. I believe adding
> a rectangle to the copper layer of a part causes problems because it
> does not have the signal name. Or maybe a rectangle does not need a
> name? But will that cause other problems such as a copper pour leaving
> a gap around it?

> The part according to TI should be like this...



> The inner rectangle has no solder mask and six 0.013" vias. The outer
> rectangle has solder mask and 0.018" vias. I don't see how to do the
> outer ones.