

## Re: TQFP handling while developing

**Source:** <http://coding.derkeiler.com/Archive/General/comp.arch.embedded/2004-05/1276.html>

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**From:** Paul E. Bennett (*peb\_at\_amleth.demon.co.uk*)

**Date:** 05/17/04

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Paul Rosen wrote:

- > *Thank you, Paul for your long answer.*
- >
- > *First I want to say, that my English is not very good. I do not know,*
- > *whether I understood everything correctly. And do not know, whether I*
- > *say everything that way, I want it to say. Sorry for this.*

My apologies but, that English is not your first language did not seem too apparent from your writing. I commend you on your accomplishment.

- >>*Either your project planning capabilities and project control are very*
- >>*naff or you are dealing with the cutting (or even bleeding) edge*
- >>*technologies. I will stay with the charitable side and consider that*
- >>*you are on the bleeding edge of developments. This then puts you in the*
- >>*realm of prototyping designs or parts of designs to ensure that you*
- >>*achieve the desired performance.*
- >
- > *This is a problem. I am the only designer in our company. The*
- > *possibilities are a bit poor. :- ( I have to solve every problem*
- > *without companion and without assistance.*
- >
- > *What is a naff project control? Or better: What makes a project control*
- > *the opposite of naff?*

"naff" is a colloquial expression (local slang) for dispicably innefctive. The term is rather derogatory but I was not implying that you were in that particular category.

- >>*cutting vs bleeding edge*
- > *Could you explain that with other words ... my limited English.*
- > *Sometimes I think, a good equipment makes your thoughts poor. I do not*
- > *really know, which side is better to switch charitable mode on or off.*
- > *;-) But the die of PLCC is too hard. Some effects maybe compensated,*
- > *but others not.*

"Cutting edge" is in the realm of being so new that it has not been done before in this context. "Bleeding edge" is a more extreme version such that

not only has it not been done before but you are doing it for the first time as a full production prospect (usually hurts more than the cutting edge)..

- >>OK, so you are already using prototyping boardlets with impedance
- >>controlled padding.
- >
- > You are speaking from the little PCBs with the controller on it?
- > Please, tell me more about "impedance controlled padding".

Often, when prototyping RF circuits, instead of creating a PCB we take a sheet of plain copper clad board. We mount our devices on small PCB's that have only the tracking for pin connection. The distance between the pin connection tracking and acts like a good capacitor to the massive copper ground-plane. The thickness of the PCB on which the pin tracking is laid and the copper ground-plane is usually such that the characteristic impedance to ground is 50 ohms. If you have a long route you can usually tack coaxial links down easily without upsetting this characteristic impedance. I have used such boardlets up to 2.5GHz in mixed RF and Digital prototyping.

The companies that make these little boardlets started doing so as a means to make their own prototyping easier. They then found a market when some of their engineers moved over to other companies. I will have to dig back in some quite old notes to find the company's details but having your local PCB manufacturer make up a batch shouldn't be too hard.

- > The analog section is divided from the digital by both grounds, which
- > goes closed to the controller as possible. The backside (two layers)
- > of the pcb is filled with ground – digital and analog divided to their
- > sections.

[%X]

- >>Be cognizant of the impedances between layers for your chosen
- >>PCB materials.
- >
- > Isn't it capacity? Please, tell me more.

Every unit length of track is an inductance. Every pair of parallel conducting surfaces is more capacitance. Together they form the complex impedances. Get to know these well.

- >>Sounds like youi may need to also consider your decoupling philosophy
- >>or your layout topologies to ensure that you minimise cross-talk and
- >>pickup. Take your time doing this.
- >
- > I think I do it. Maybe there are some points, which I do not know.I
- > use two or more grounds.

Keep analogue and digital ground separate from each other and route both by the shortest sensible route. Making the digital ground a full plane on your digital section of the PCB will reduce the inductance of the copper and increase the capacitance to the logic supply rails (a good thing). You might also find that digital capacitive power busbar rails are useful (are these still around?).

- > .... *Every section is screened by its own ground.*
- > *Critical signals are double screened with its own signal, hardened by*
- > *an amp and then with its ground. Astral wiring as most as possible..*
- > *Very critical points (high impedance) are divided by gaps in the PCB*
- > *or sometimes wired in the air. In extreme situations they are*
- > *sealed from the humidity. I use screen-sheets. I always use*
- > *kelvin-design for critical measurements. I decouple wires with high*
- > *and low current. The thermo effect of a soldering joint is annihilated*
- > *by an inverse one, if disturbing. I take care of the route of every*
- > *lead. I decouple switched high-voltage leads by resistances near to*
- > *the switches, to avoid broadcast. This all for PCB route and real wire*
- > *route. I hope I did not forget anything. Anything more to do?*

Sounds like you already have a lot of the right techniques in place. You may also like to consider the benefit of adding metal screen cans over some parts of your circuitry (connected to ground potential) to quieten things down a bit. I know that it restricts access but adding a few well placed test points will assist with troubleshooting without having to remove the cans.

- > *But there is the mechanical process equipment, which is not always*
- > *asked me. And sometimes the design of the electronic is made by*
- > *optical aspects. They do not want the electronic to "get cluttered" to*
- > *different places of the equipment, which would be useful for good*
- > *decoupling. And sometimes the mechanical equipment lets you not do,*
- > *what would be good to avoid crosstalk and pickup. Although this, you*
- > *have to provide a working design. And that could make problems when*
- > *changing a working prototype layout because TQFP. But it helps, what*
- > *you said above.*

I suspect that you have considered distributing the separate elements of the system amongst the equipment to improve signal to noise ratios of the analogue signals. Where this is possible it will certainly help. However, it does change the architecture of your system and you need to think a bit about sanity checking the distributed modules.

There are many reasons not to distribute the sensor and control elements of your system. Some of these relate to the environment out on the equipment (is it very harsh or restricted). You can only resolve that with your mechanical colleagues.

- >>> *And what is about emulation, when the processor is soldered into the*
- >>> *board?*
- >

> *Still unanswered*

I may have missed what you are asking here. I presume you were asking about the difference between what you see in emulation software (like PSPICE etc) and the reality of the real components. If this is the question then the answer is that the models in PSPICE are only based on the theoretical equivalent circuit network that characterises each component. The models can be improved if you have better actual or experimental data that you can trust in a variety of situations. The better data can take quite a while to develop though so most of us will consider the supplied models good enough for most purposes. However, where you can see a difference between the model and the actuality you can revisit the model and alter it until it does match your observed data. I have done this with PSPICE myself for some IGBT and TRANSORB models that I had to adapt from other less ideal components.

>>*Relax a little more and don't get so flustered. Sit and think a bit more about what you are doing and whether there may be better approaches. I haven't followed this thread from the beginning but I am sure that pausing for thought to think what others have said here will help you resolve the problems you feel you are having.*

>

> *They said, that I could program the controllers in-circuit. I know that. This helps only for the software, but not for the hardware.*

Very true. No amount of programming effort will eliminate the hardware shortfalls. Get the hardware platform right in terms of stability although I would expect you to have the major structure (not code) of your software fairly well planned out already.

> *Maybe, I should calm down But that does not change this fact: The die of PLCC makes problems for analog-development not easier. And I am quite safe, that this bothers not only me.*

I am sure you are right. With over thirty years of experience in a wide range of system problems I have come across plenty of problems foisted on the development team by others (not only disti's) We just learn to suck in a deep breath, count to ten and then just think quietly to ourselves "here we go again!!". Taking such problems in a calm, collected manner and working through the individual problems in as logical a process of elimination as you can muster will lead to you discovering the right solution to your problems. However, be honest about your problems to your line management as sometimes they appreciate it (even if they don't like the news).

To the others, with much shorter responses, I think that you should offer some real practical advice to Paul Rosen. As one who has not had any experience with PIC's or Microchip (apart from getting unwanted mailshots from them) I can only speak in generalities to try to help him. Mixed signal designs can be real bitches at times and impedance

comp.arch.embedded: Re: TQFP handling while developing

issues, correct grounding and board layout issues specific to this chip  
need to be aired.

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