

Re: OV7620 image sensor interface with FPGA headache

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On Friday, in article

<eb85bd6eab936116056f3a4830038d87@localhost.talkaboutelectronicsequipment.com>
dwmunandar@yahoo.com "dalle002" wrote:

>Dear helpers,

>

>Your inputs were awesome. I made sure the I2C was enabled, put a 4k7
>pullup resistor and make sure the timing specifications are met and BAM!
>it works! I got the acknowledge signals and the PCLK frequency has doubled
>to 27MHZ. I was jumping up and down for a while in gladness. Thank you all
>for your help. Probably my biggest mistake is the 300k resistor I used.

Glad to see you have made progress...

>Now I still need further help on sending the image to the VGA monitor. Did
>anyone has succesfully send the digital image directly to a monitor
>without any need of storing the image in a memory?

I think you will find that difficult, because the first paragraph of the data sheet I have states

"The devices incorporate a 640 x 480 image array capable of operating at up to 30 frames per second."

So it is NOT possible to get VGA resolution continuously at 60fps. INTERLACED at 60fps (NTSC timings) should be possible.

QVGA at 60fps is possible.

>I tried to store the pixel information in registers that is output to the
>color signals to the monitor. I noticed with progressive 16-bit mode, the
>UV channel output G and R values in sequence, and the Y channel output B
>and G values.

That is because the device only has 2 A/Ds and that is primarily meant for still images or QVGA 'movies' as progrssive scan in digital format

to be processed externally. It is NOT meant as a standard video camera. This is one of the standard modes which you will have to control by the I2C to change to any other format.

> I noticed that the register go some values but if I use the
> VSYNC and HREF signal from the camera sent directly to the monitor,
> nothing showed up.

Because you have data and timing for basically still image capture, not as a continuous progressive scan video camera. You will need a video (not PC graphics) monitor to display an interlaced mode image.

> I also use the FPGA to count numbers of HSYNC in a frame. The FPGA counted
> about 424 HREF signals plus minus 10 more. I'm wondering how come the
> number is not consistent? And why is it not close to 492 (I'm expecting
> 492 lines for VGA output).
>
> I'm wondering if this is because the sampling clock my FPGA use (50MHz) is
> not sufficient to sample the pixel information (13MHz) for progressive,
> RGB, 16-bit mode? Would anyone recommend taking out the camera's
> oscillator, connect the JP1 jumper and give the camera and external clock
> from the FPGA?

Clocking from the FPGA is an option but understand the timing and max clock of 30MHz that must drive the camera, perhaps sort timings for 25MHz clock to camera. Your discrepancies depend on how you are clocking the count and saving results and reading the results. Are you clearing the count during vertical and missing the HSYNCs during vertical sync or worse still during vertical blanking.

> I also noticed a discrepancy in the camera's data sheets. It says that if
> it were to be set as a slave with an external clock provided, the VSYNC
> signal must be provided to the camera. The VSYNC signal must follow the
> formula: $525 * 2 * 858 * Tclk$ – which will only give about 30Hz/fps for an 25MHz
> clock input? I need a 60Hz output for the monitor. Currently with the
> camera's original oscillator, I observed 60Hz VSYNC signal given by the
> camera. Why the disagreement?

Understand the differences between frames and fields, in relation to progressive and interlaced scan.

Interlaced scan gives 30 FRAMES per second consisting of
60 FIELDS, hence 60Hz VSYNC.

Progressive scan gives 30 FRAMES per second hence 30Hz VSYNC

The data sheet is badly written (appears to have been translated via 10 languages and back again) and has a few typos in it.

> Can anyone offer me any help on these questions? Any amount of input will
> be appreciated.

comp.arch.embedded: Re: OV7620 image sensor interface with FPGA headache

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>*Thanks ahead.*

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