

# DDR SDRAM with Xilinx Virtex 2 on self designed PCB

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Hello,

last week I started the development and design of a PCB with an FPGA (Xilinx Virtex 2) and two DDR-SDRAMs in parallel. No big deal, I thought, keeping in mind the most obvious design rules, i.e. combining the adress lines and separating the data and strobe (DQS) lines. But now I came across the many other signals there are, e.g. the clock signals, S0 and S1, CAS, RAS, WE, etc. My first idea was to also combine them for both modules. Lately I wondered if I am right with that assumption?

Regards, Elmo