

Re: Interest in AVR+MSP430 "general purpose" proto board?

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- *From:* Jim Granville <no.spam@xxxxxxxxxxxxxxxxxxxxxxxxxxxx>
 - *Date:* Fri, 20 Apr 2007 08:43:41 +1200
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larwe wrote:

On Apr 19, 4:48 am, Clifford Heath <n...@xxxxxxxxxxxxxxxxxxxx> wrote:

Nice idea, BTW. Would be nice with a CPLD as Jim suggested.

All right, all right, what is with the CPLD? CPLD talk is not going to make it into my book, but just supposing I were to add it to this board, how would you want it wired? All the pins coming to headers, or half the I/Os going to a micro and the other half to a header?

OK, here is one suggestion:

Wire 4 CPLD pins to the uC(s), as SPI

SPI_DI
SPI_DO
SPI_SS
SPI_CK

and some of the others can go to pin headers,
– you can work out from their names, what they
are used for, and some header candidates :)

Pin Name Resource/Direction

43 on LCD_RWn Dge--
44 on LCD_RS Dge--
1 -- TDI INPUT
2 PT DB6 Dge--
3 PT DB5 Dge--
5 PT DB7 Dge--
6 PT DB4 Dge--
7 -- TMS INPUT
8 PT DB1 Dge--

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10 PT DB3 Dge--
11 PT DB2 Dge--
12 PT DB0 Dge--
13 on LCD_E Tg-g-
14 --- SPI_DI INPUT
15 on SPI_DO C-----
32 --- TDO C-----
26 --- TCK INPUT
39 SPI_SS INPUT << Locked Pin
37 SPI_CK INPUT << Locked Pin

Spares could go to backlight, and buttons – depends on board space really.

and the programming pin header – IDC10

IDC10 CPLD pin

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JTAG.1 S PIN26_C62_TCK_B
JTAG.2 S GND
JTAG.3 S PIN32_C73_TDO
JTAG.4 S VCCIO
JTAG.5 S PIN7_C15_TMS_B
JTAG.6 E PIN40_C90_GCLK2B
JTAG.7 E PIN39_C89_GCLRB
JTAG.8 E PIN37_C87_GCLK1B
JTAG.9 S PIN1_C4_TDI_B
JTAG.10 E GND_OR_VCCINT Jumper Selected. Allows JTAG unlock, Some PCBs GND.10

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