

Re: Question about strange flash problem

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- *From:* "andrew queisser" <andrewdotqueisser@xxxxxx>
 - *Date:* Mon, 23 Apr 2007 11:44:31 -0700
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"Arlet" <usenet+5@xxxxxxxxxxx> wrote in message
<news:1177353290.225359.291360@xx>

On Apr 23, 6:57 pm, "andrew queisser" <andrewdotqueis...@xxxxxx>
wrote:

Hi all,

I'm seeing a strange bug with a flash chip. So far it's isolated but I was wondering if anyone has opinions about what might be happening here:

Chip: Spansion
32MBithttp://www.spansion.com/datasheets/s29a1032d_00_a8_e.pdf

When I program certain sectors (3f8000,3fa000,3fc000,3fe000) they act like RAM. I can write data and read data back but when I power cycle the device the data is back to 0xFFFF...

I can think of a few explanations but I don't know enough about the inner workings of flash to know which ones to eliminate:

- 1) The chip is defective and acts like a RAM chip on those sectors
- 2) The sectors in question are write-protected and act therefore act like RAM
- 3) There's a defect on our PCB and I actually am writing to the SRAM chip sharing the address bus
- 4) There's a defect on the chip that causes the sectors to be erased each time the device powers up

Some background:

- It's an FPGA based system with flash and SRAM sharing the bus.
- We don't have any high voltages hooked up to the flash chip so our only way of programming are the in-system CFI routines.
- The programming routines include a normal SRAM-like write cycle at the end

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so that would explain how it could look like SRAM

– So far only one of several devices exhibit the problem, all others work fine.

Does your system have a cache ? It sounds like that part of the memory is cached.

I would rule out options 1 and 2. Option 3 may be possible. Number 4 is unlikely. Can you do a soft reset of the CPU alone to rule out option 4 ? You could use a scope on the RAM/Flash control lines (CS#, OE#, WE#) and see if the SRAM is addressed instead of the Flash during programming.

Thanks for the tips.

We don't have data cache on our design right now, just instruction cache.

When I do a soft reset of the CPU the flash contents stay unchanged, it's definitely something related to the power-up phase. The idea of looking at the CS,OE and WE lines is a good one. Since this is an FPGA I can use the built-in signal analyzer to set that up. Otherwise it would be hard to probe those lines.

So it seems Option 3 is most likely right now. In addition to probing I'll do a memcheck to see if I find the pattern I program into flash anywhere in the memory map...

Thanks again,
Andrew

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